Your search matched **1** of **1041798** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enteri new one in the text box.

emulation and debug and trigger Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

1 **A comprehensive analyzer for the JIAWG high speed data bus**
Archer, H.S.;
Aerospace and Electronics Conference, 1990. NAECON 1990., Proceedings of IEEE 1990 National , 21-25 May 1990
Pages:174 - 182 vol.1

[Abstract] [PDF Full-Text (824 KB)] **IEEE CNF**

Your search matched **3** of **1041798** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enteri new one in the text box.

emulation and debug and clock Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

---

1 **Pattern generator card, emulation, and debug**
Dunn, S.M.; Balazich, D.G.; Lange, L.K.; Montillo, C.C.;
VLSI Test Symposium, 1993. Digest of Papers., Eleventh Annual 1993 IEEE , April 1993
Pages:358 - 360

[Abstract] [PDF Full-Text (208 KB)] **IEEE CNF**

---

2 **A hardware accelerator for DSP system design: University of Tehran Hardware Emulator (UTDHE)**
Mahdiany, H.R.; Hormati, A.; Fakhraie, S.M.;
Microelectronics, 2001. ICM 2001 Proceedings. The 13th International Confere on , 29-31 Oct. 2001
Pages:141 - 144

[Abstract] [PDF Full-Text (408 KB)] **IEEE CNF**

---

3 **A 200 MHz 1.2 W 1.4 GFLOPS microprocessor with graphic operation**
Nishii, O.; Arakawa, F.; Ishibashi, K.; Nakano, S.; Shimura, T.; Suzuki, K.; Tachibana, M.; Totsuka, Y.; Tsunoda, T.; Uchiyama, K.; Yamada, T.; Hattori, Maejima, H.; Nakagawa, N.; Narita, S.; Seki, M.; Shimazaki, Y.; Satomura, R Takasuga, T.; Hasegawa, A.;
Solid-State Circuits Conference, 1998. Digest of Technical Papers. 45th ISSCC 1998 IEEE International , 5-7 Feb. 1998
Pages:288 - 289, 447

[Abstract] [PDF Full-Text (1216 KB)] **IEEE CNF**

Your search matched **15** of **1041798** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enteri new one in the text box.

emulation and debug Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

---

1 **Pattern generator card, emulation, and debug**
Dunn, S.M.; Balazich, D.G.; Lange, L.K.; Montillo, C.C.;
VLSI Test Symposium, 1993. Digest of Papers., Eleventh Annual 1993 IEEE , April 1993
Pages:358 - 360

[Abstract] [PDF Full-Text (208 KB)] **IEEE CNF**

---

2 **Using background modes for testing, debugging and emulation of microcontrollers**
Melear, C.;
WESCON/97. Conference Proceedings , 4-6 Nov. 1997
Pages:90 - 97

[Abstract] [PDF Full-Text (444 KB)] **IEEE CNF**

---

3 **Design and implementation of ad hoc network protocol debugging environment**
ZhiFeng Zhao; ShaoRen Zheng;
Military Communications Conference, 2001. MILCOM 2001. Communications f Network-Centric Operations: Creating the Information Force. IEEE , Volume: 2 , 28-31 Oct. 2001
Pages:855 - 859 vol.2

[Abstract] [PDF Full-Text (141 KB)] **IEEE CNF**

---

4 **Emulation: Debug it in the lab-not on the floor**
Schiess, C.;
Simulation Conference, 2001. Proceedings of the Winter , Volume: 2 , 9-12 D 2001
Pages:1463 - 1465 vol.2

[Abstract] [PDF Full-Text (386 KB)] **IEEE CNF**

5 **Si-emulation: system verification using simulation and emulation**
Zan Yang; Byeong Min; Gwan Choi;
Test Conference, 2000. Proceedings. International , 3-5 Oct. 2000
Pages:160 - 169

[Abstract] [PDF Full-Text (700 KB)] **IEEE CNF**

6 **Tool reusable for DSP system emulation and board production testin**
Gonzales, D.R.;
Northcon/96 , 4-6 Nov. 1996
Pages:306 - 311

[Abstract] [PDF Full-Text (492 KB)] **IEEE CNF**

7 **A hardware accelerator for DSP system design: University of Tehran Hardware Emulator (UTDHE)**
Mahdiany, H.R.; Hormati, A.; Fakhraie, S.M.;
Microelectronics, 2001. ICM 2001 Proceedings. The 13th International Confere on , 29-31 Oct. 2001
Pages:141 - 144

[Abstract] [PDF Full-Text (408 KB)] **IEEE CNF**

8 **Debugging aids for systems-on-a-chip**
Bannatyne, R.;
WESCON/98 , 15-17 Sept. 1998
Pages:107 - 111

[Abstract] [PDF Full-Text (340 KB)] **IEEE CNF**

9 **Emulation of a material delivery system**
LeBaron, T.; Thompson, K.;
Simulation Conference Proceedings, 1998. Winter , Volume: 2 , 13-16 Dec. 19
Pages:1055 - 1060 vol.2

[Abstract] [PDF Full-Text (476 KB)] **IEEE CNF**

10 **A 200 MHz 1.2 W 1.4 GFLOPS microprocessor with graphic operatio unit**
Nishii, O.; Arakawa, F.; Ishibashi, K.; Nakano, S.; Shimura, T.; Suzuki, K.; Tachibana, M.; Totsuka, Y.; Tsunoda, T.; Uchiyama, K.; Yamada, T.; Hattori, Maejima, H.; Nakagawa, N.; Narita, S.; Seki, M.; Shimazaki, Y.; Satomura, R Takasuga, T.; Hasegawa, A.;
Solid-State Circuits Conference, 1998. Digest of Technical Papers. 45th ISSCC 1998 IEEE International , 5-7 Feb. 1998
Pages:288 - 289, 447

[Abstract] [PDF Full-Text (1216 KB)] **IEEE CNF**

11 **Visual dynamic environment for distributed systems**
Di Gesu, V.; Isgro, F.; Lenzitti, B.; Tegolo, D.;
Computer Architectures for Machine Perception, 1995. Proceedings. CAMP '95 20 Sept. 1995
Pages:359 - 366

[Abstract] [PDF Full-Text (836 KB)] IEEE CNF

---

12 **Using background modes for testing, debugging and emulation of microcontroller**
Melear, C.;
Southcon/95. Conference Record , 7-9 March 1995
Pages:84 - 89

[Abstract] [PDF Full-Text (356 KB)] IEEE CNF

---

13 **A validation strategy for embedded core ASICs**
Hasslen, R.J.; Zafar, N.;
ASIC Seminar and Exhibit, 1990. Proceedings., Third Annual IEEE , 17-21 Sep 1990
Pages:P5/3.1 - P5/3.2

[Abstract] [PDF Full-Text (176 KB)] IEEE CNF

---

14 **A comprehensive analyzer for the JIAWG high speed data bus**
Archer, H.S.;
Aerospace and Electronics Conference, 1990. NAECON 1990., Proceedings of IEEE 1990 National , 21-25 May 1990
Pages:174 - 182 vol.1

[Abstract] [PDF Full-Text (824 KB)] IEEE CNF

---

15 **Design for test in a custom 8-bit microcontroller**
Jones, M.;
Guaranteeing the Reliability of Automotive Electronics, IEE Colloquium on , 18 1988
Pages:7/1 - 7/6

[Abstract] [PDF Full-Text (124 KB)] IEE CNF

Your search matched **1** of **1041798** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enteri new one in the text box.

emulation and debug and ic Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

---

1 **A 200 MHz 1.2 W 1.4 GFLOPS microprocessor with graphic operation**
Nishii, O.; Arakawa, F.; Ishibashi, K.; Nakano, S.; Shimura, T.; Suzuki, K.; Tachibana, M.; Totsuka, Y.; Tsunoda, T.; Uchiyama, K.; Yamada, T.; Hattori, Maejima, H.; Nakagawa, N.; Narita, S.; Seki, M.; Shimazaki, Y.; Satomura, R Takasuga, T.; Hasegawa, A.;
Solid-State Circuits Conference, 1998. Digest of Technical Papers. 45th ISSCC 1998 IEEE International , 5-7 Feb. 1998
Pages:288 - 289, 447

[Abstract] [PDF Full-Text (1216 KB)] **IEEE CNF**

Your search matched **0** of **1041798** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enteri new one in the text box.

emulation and debug and ic and testability Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

---

Results:
No documents matched your query.

Your search matched **0** of **1041798** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enteri new one in the text box.

swoboda and debug Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

---

Results:
No documents matched your query.

Your search matched **0** of **1041798** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enteri new one in the text box.

emulation and debug and oscillator Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

---

Results:
No documents matched your query.

Your search matched **19** of **1041798** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enteri new one in the text box.

swoboda Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

---

1 **The polar co-ordinate magnetic measuring system for the axial field spectrometer magnet at the ISR-CERN**
Swoboda, D.;
Magnetics, IEEE Transactions on , Volume: 17 , Issue: 5 , Sep 1981
Pages:2125 - 2128

[Abstract] [PDF Full-Text (584 KB)] IEEE JNL

---

2 **A low-noise monolithically integrated 1.5 Gb/s optical receiver in 0. /spl mu/m BiCMOS technology**
Swoboda, R.; Zimmermann, H.;
Selected Topics in Quantum Electronics, IEEE Journal of , Volume: 9 , Issue: 2 , March-April 2003
Pages:419 - 424

[Abstract] [PDF Full-Text (928 KB)] IEEE JNL

---

3 **Status of the ALICE magnet system**
Swoboda, D.; Leistam, L.; Pigni, L.; Cacaut, D.; Kochournikov, E.; Vodopiano
Applied Superconductivity, IEEE Transactions on , Volume: 12 , Issue: 1 , Mar 2002
Pages:432 - 437

[Abstract] [PDF Full-Text (283 KB)] IEEE JNL

---

4 **The dipole magnet design for the ALICE DiMuon arm spectrometer**
Akishin, P.; Anischenko, N.; Blinov, N.; Boguslavsky, I.; Cacaut, D.; Danilov, Datskov, V.; Golubitsky, O.; Kalimov, A.; Kochournikov, E.; Lyubimtsev, A.; Makarov, A.; Mikhailov, K.; Olex, I.; Popov, V.; Semashko, S.; Shabunov, A.; Shishov, Y.; Shurygin, A.; Shurygina, M.; Sissakian, A.; Swoboda, D.; Vodopi A.;
Applied Superconductivity, IEEE Transactions on , Volume: 12 , Issue: 1 , Mar 2002

Pages:399 - 402

[Abstract] [PDF Full-Text (233 KB)] IEEE JNL

---

5 **Design and status of the dipole spectrometer magnet for the ALICE experiment**
Swoboda, D.; Barlenev, V.; Bogouslavski, I.; Datskov, V.; Koshurnikov, E.; Shabunov, A.; Shishov, Y.; Vodopianov, A.;
Applied Superconductivity, IEEE Transactions on , Volume: 10 , Issue: 1 , Mar 2000
Pages:411 - 414

[Abstract] [PDF Full-Text (188 KB)] IEEE JNL

---

6 **A proposed scalable parallel open architecture data acquisition syst for low to high rate experiments, test beams and all SSC detectors**
Barsotti, E.; Booth, A.; Bowden, M.; Swoboda, C.; Lockyer, N.; VanBerg, R.;
Nuclear Science, IEEE Transactions on , Volume: 37 , Issue: 3 , June 1990
Pages:1216 - 1221

[Abstract] [PDF Full-Text (576 KB)] IEEE JNL

---

7 **A high-rate Fastbus silicon strip readout system**
Swoboda, C.; Barsotti, E.; Bowden, M.; Christian, D.; DeMaat, R.; Fachin, M.; Gonzalez, H.; Hance, R.; Haldeman, M.; Hoff, J.; Larwill, M.; Rotolo, C.; Trend R.; Trepstow, K.; Urish, J.; Walsh, D.; Yarema, R.; Zimmerman, T.;
Nuclear Science, IEEE Transactions on , Volume: 37 , Issue: 2 , April 1990
Pages:342 - 346

[Abstract] [PDF Full-Text (400 KB)] IEEE JNL

---

8 **FASTBUS standard fiber optic data transfer link**
Swoboda, C.; Barsotti, E.; Moore, G.; Pordes, R.; Downing, R.; Watase, Y.; Nomachi, M.;
Nuclear Science, IEEE Transactions on , Volume: 36 ; Issue: 1 , Feb. 1989
Pages:774 - 779

[Abstract] [PDF Full-Text (440 KB)] IEEE JNL

---

9 **2.5 Gbit/s silicon receiver OEIC with large diameter photodiode**
Swoboda, R.; Zimmermann, H.;
Electronics Letters , Volume: 40 , Issue: 8 , 15 April 2004
Pages:505 - 506

[Abstract] [PDF Full-Text (215 KB)] IEE JNL

---

10 **Speed-enhanced OEIC with voltage-up-converter**
Swoboda, R.; Knorr, I.; Zimmermann, H.;
Electronics Letters , Volume: 39 , Issue: 1 , 9 Jan. 2003
Pages:112 - 113

[Abstract] [PDF Full-Text (276 KB)] IEE JNL

---

11 **A low-noise 1.8Gbps bipolar OEIC**
Swoboda, R.; Zimmermann, H.;
European Solid-State Circuits, 2003. ESSCIRC '03. Conference on , 16-18 Sep

2003
Pages:341 - 344

[Abstract] [PDF Full-Text (534 KB)] IEEE CNF

---

12 **Using intranet technology to access valuable information in a clinic environment fast and efficiently**
Fuckner, T.; Swoboda, N.C.; Adelhard, K.;
Intelligent Information Systems, 1997. IIS '97. Proceedings , 8-10 Dec. 1997
Pages:24 - 26

[Abstract] [PDF Full-Text (200 KB)] IEEE CNF

---

13 **Speed-enhanced OEIC with area-efficient charge pump and shunt regulator**
Swoboda, R.; Knorr, J.; Zimmermann, H.;
Electron Devices for Microwave and Optoelectronic Applications, 2003. EDMO The 11th IEEE International Symposium on , 17-18 Nov. 2003
Pages:66 - 70

[Abstract] [PDF Full-Text (347 KB)] IEEE CNF

---

14 **On Surface Hot-Film Applications in Laminar-Turbulent Flows**
Swoboda, M.; Haselbach, F.; Wald, L.; Nitsche, W.;
Instrumentation in Aerospace Simulation Facilities, 1993. ICIASF '93 Record. International Congress on , September 20-23, 1993
Pages:17_1 - 17_8

[Abstract] [PDF Full-Text (1876 KB)] IEEE CNF

---

15 **Results from a data acquisition system prototype project using a switch-based event builder**
Black, D.; Bowden, M.; Andresen, J.; Barsotti, E.; Baumbaugh, A.; Booth, A.; Cancelo, G.; Esterline, D.; Knickerbocker, K.; Kwarciany, R.; Moore, G.; Patri Swoboda, C.; Treptow, K.; Tevizo, O.; Urish, J.; VanConant, R.; Walsh, D.;
Nuclear Science Symposium and Medical Imaging Conference, 1991., Confere Record of the 1991 IEEE , 2-9 Nov. 1991
Pages:833 - 837 vol.2

[Abstract] [PDF Full-Text (292 KB)] IEEE CNF

---

1 2 Next

Your search matched **19** of **1041798** documents.
A maximum of **500** results are displayed, **15** to a page, sorted by **Relevance Descending** order.

Refine This Search:
You may refine your search by editing the current search expression or enteri new one in the text box.

swoboda Search

☐ Check to search within this result set

Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

---

16 **Status of the silicon strip high-rate FASTBUS readout system**
Gonzalez, H.; Barsotti, E.; Bowden, M.; Christian, D.; Chramowicz, J.; Fachin Haldeman, M.; Hoff, J.; Holmes, S.; Rotolo, C.; Romero, A.; Slimmer, D.; Swoboda, C.; Trendler, R.; Urish, J.; Yarema, R.; Zimmerman, T.; Zimmerma S.; Kowald, W.; MacManus, A.; Recagni, M.; Segal, J.; Spentzouris, P.;
Nuclear Science Symposium and Medical Imaging Conference, 1991., Confere Record of the 1991 IEEE , 2-9 Nov. 1991
Pages:747 - 752 vol.2

[Abstract] [PDF Full-Text (436 KB)] **IEEE CNF**

---

17 **Shock detection on airfoils by means of piezo foil- and hot film arra**
Swoboda, M.; Nitsche, W.; Suttan, J.;
Instrumentation in Aerospace Simulation Facilities, 1991. ICIASF '91 Record., International Congress on , 27-31 Oct. 1991
Pages:284 - 294

[Abstract] [PDF Full-Text (896 KB)] **IEEE CNF**

---

18 **The new vacuum control system for the SPS**
Swoboda, D.;
Particle Accelerator Conference, 1991. 'Accelerator Science and Technology'., Conference Record of the 1991 IEEE , 6-9 May 1991
Pages:1516 - 1518 vol.3

[Abstract] [PDF Full-Text (268 KB)] **IEEE CNF**

---

19 **Hot-wire, hot-film and surface hot-film applications in strongly temperature loaded flows**
Thunker, R.; Nitsche, W.; Swoboda, M.;
Instrumentation in Aerospace Simulation Facilities, 1989. ICIASF '89 Record., International Congress on , 18-21 Sept. 1989
Pages:434 - 442

Nothing Found

Your search for **+emulation +and +debug +and +clock +and +trigger +and +oscillator** did not return any results.

You may want to try an Advanced Search for additional options.

Please review the Quick Tips below or for more information see the Search Tips.

Quick Tips

- Enter your search terms in lower case with a space between the terms.

  ```
  sales offices
  ```

  You can also enter a full question or concept in plain language.

  ```
  Where are the sales offices?
  ```

- Capitalize proper nouns to search for specific people, places, or products.

  ```
  John Colter, Netscape Navigator
  ```

- Enclose a phrase in double quotes to search for that exact phrase.

  ```
  "museum of natural history" "museum of modern art"
  ```

- Narrow your searches by using a + if a search term must appear on a page.

  ```
  museum +art
  ```

- Exclude pages by using a - if a search term must not appear on a page.

  ```
  museum -Paris
  ```

Combine these techniques to create a specific search query. The better your description of the information you want, the more relevant your results will be.

```
museum +"natural history" dinosaur -Chicago
```

Terms used
emulation and **debug** and **clock** and **trigger** and **trace**

Found **35** of **51** searched out of **807,214**.

Sort results by: relevance
Display results: expanded form

Save results to a Binder
Search Tips
☐ Open results in a new window

Try an Advanced Search
Try this search in The Digital Library

Results 1 - 20 of 35 Result page: **1** 2 next

Relevance scale ■■■■■

1 Trace-based mobile network emulation
Brian D. Noble, M. Satyanarayanan, Giao T. Nguyen, Randy H. Katz
October 1997 **ACM SIGCOMM Computer Communication Review , Proceedings of the ACM SIGCOMM '97 conference on Applications, technologies, architectures, and protocols for computer communication**, Volume 27 Issue 4

Full text available: pdf(1.61 MB) Additional Information: full citation, abstract, references, citings, index terms

Subjecting a mobile computing system to wireless network conditions that are realistic yet reproducible is a challenging problem. In this paper, we describe a technique called *trace modulation* that re-creates the observed end-to-end characteristics of a real wireless network in a controlled and repeatable manner. Trace modulation is transparent to applications and accounts for all network traffic sent or received by the system under test. We present results that show that it is indeed cap ...

2 Summary of ACM/ONR workshop on parallel and distributed debugging
January 1992 **ACM SIGOPS Operating Systems Review**, Volume 26 Issue 1

Full text available: pdf(1.31 MB) Additional Information: full citation, citings, index terms

3 First International Workshop on Persistence and Java
Malcolm Atkinson, Mick Jordan
November 1996 Technical Report, Sun Microsystems, Inc.

Full text available: pdf(1.54 MB) Additional Information: full citation, abstract

These proceedings record the First International Workshop on Persistence and Java, which was held in Drymen, Scotland in September 1996. The focus of this workshop was the relationship between the Java languages and long-term data storage, such as databases and orthogonal persistence. There are many approaches being taken, some pragmatic and some guided by design principles. If future application programmers building large and long-lived systems are to be well-supported, it is essential that the ...

4 The Role of Modeling and Asynchronous Distributed Simulation in Analyzing Complex Systems of the Future
Sumit Ghosh
July 2002 **Information Systems Frontiers**, Volume 4 Issue 2

Full text available: Publisher Site Additional Information: full citation, abstract, index terms

The word simulate implies to imitate or to mimic while the word modeling refers to a small

object, usually built to scale, that represents some existing object. Although the art of mimicking and modeling may be traced back to the beginning of civilization, with the emergence of computers, a few decades ago, the art of modeling and simulation experienced a remarkable transformation. The computational intelligence of the computer imparted the ability to encapsulate and simulate specific charact ...

Keywords: complex processes, distributed processing, modeling, physical and natural systems, real-world problems, simulation

5 Distributed systems - programming and management: On remote procedure call

Patrícia Gomes Soares

November 1992 **Proceedings of the 1992 conference of the Centre for Advanced Studies on Collaborative research - Volume 2**

Full text available: pdf(4.52 MB) Additional Information: full citation, abstract, references

The Remote Procedure Call (RPC) paradigm is reviewed. The concept is described, along with the backbone structure of the mechanisms that support it. An overview of works in supporting these mechanisms is discussed. Extensions to the paradigm that have been proposed to enlarge its suitability, are studied. The main contributions of this paper are a standard view and classification of RPC mechanisms according to different perspectives, and a snapshot of the paradigm in use today and of goals for t ...

6 Logic synthesis and mapping: Verifying the correctness of FPGA logic synthesis algorithms

Boris Ratchev, Mike Hutton, Gregg Baeckler, Babette van Antwerpen

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(146.65 KB) Additional Information: full citation, abstract, references, index terms

Though verification is significantly easier for FPGA-based digital systems than for ASIC or full-custom hardware, there are nonetheless many places for errors to occur.In this paper we discuss the verification problem for FPGAs and describe several methods for verifying end-to-end correctness of synthesis algorithms, a particularly complex portion of the CAD flow. Though the primary contribution of this paper is the analysis of the overall problem, we also give an algorithm for the automatic gen ...

Keywords: FPGA, programmable logic, synthesis, test, verification

7 Prototyping, verification, and test: High-level modeling and FPGA prototyping of microprocessors

Joydeep Ray, James C. Hoe

February 2003 **Proceedings of the 2003 ACM/SIGDA eleventh international symposium on Field programmable gate arrays**

Full text available: pdf(148.95 KB) Additional Information: full citation, abstract, references, index terms

Emerging high-level hardware description and synthesis technologies in conjunction with field-programmable gate arrays (FPGAs) have significantly lowered the threshold for hardware development. Opportunities exist to integrate these technologies into a tool for exploring and evaluating microarchitectural designs. This paper presents a case study in developing the synthesizable high-level model of a superscalar processor and producing a working prototype in FPGA. Using an experimental operation-c ...

Keywords: FPGA, evaluation, microarchitecture, microprocessor, operation-centric, prototyping

8

An RTL Abstraction Technique for Processor Microarchitecture Validation and Test

Generation
Jian Shen, Jacob A. Abraham
February 2000 **Journal of Electronic Testing: Theory and Applications**, Volume 16 Issue 1-2

Full text available: Publisher Site Additional Information: full citation, abstract, index terms

Design validation is becoming more and more a bottleneck in the microprocessor design process. The difficulty of validation stems from the complexity of the design, which requires searching an enormous space to check correctness. This is exacerbated by features for enhancing performance, such as pipelines, which are becoming common in most microprocessors. This paper describes a new abstraction technique to handle this problem. Our solution is a novel method to identify the control sta ...

Keywords: coverage measurement, microprocessor design validation, test generation

9 Special session on on-chip multi-processing: Design experience of a chip multiprocessor merlot and expectation to functional verification
Satoshi Matsushita
October 2002 **Proceedings of the 15th international symposium on System Synthesis**

Full text available: pdf(797.44 KB) Additional Information: full citation, abstract, references, index terms

We have fabricated a Chip Multiprocessor prototype code-named Merlot to proof our novel speculative multithreading architecture. On Merlot, multiple threads provide wider issue window beyond ordinal instruction level parallel (ILP) processors like superscalar or VLIW. With the architecture, we estimate 3.0 times speedup against single processing elements (PE) on speech recognition code and IDCT code with four PEs. Merlot integrates on-chip devices, PCI interface, and SDRAM interfaces. We have en ...

Keywords: CMP, chip multiprocessor, deign experience, functional verification, speculative multithreading

10 Virtual machines: ReVirt: enabling intrusion analysis through virtual-machine logging and replay
George W. Dunlap, Samuel T. King, Sukru Cinar, Murtaza A. Basrai, Peter M. Chen
December 2002 **ACM SIGOPS Operating Systems Review**, Volume 36 Issue SI

Full text available: pdf(1.56 MB) Additional Information: full citation, abstract, references, citings

Current system loggers have two problems: they depend on the integrity of the operating system being logged, and they do not save sufficient information to replay and analyze attacks that include any non-deterministic events. ReVirt removes the dependency on the target operating system by moving it into a virtual machine and logging below the virtual machine. This allows ReVirt to replay the system's execution before, during, and after an intruder compromises the system, even if the intruder rep ...

11 Fast detection of communication patterns in distributed executions
Thomas Kunz, Michiel F. H. Seuren
November 1997 **Proceedings of the 1997 conference of the Centre for Advanced Studies on Collaborative research**

Full text available: pdf(4.21 MB) Additional Information: full citation, abstract, references, index terms

Understanding distributed applications is a tedious and difficult task. Visualizations based on process-time diagrams are often used to obtain a better understanding of the execution of the application. The visualization tool we use is Poet, an event tracer developed at the University of Waterloo. However, these diagrams are often very complex and do not provide the user with the desired overview of the application. In our experience, such tools display repeated occurrences of non-trivial commun ...

12

The transport layer: tutorial and survey
Sami Iren, Paul D. Amer, Phillip T. Conrad
December 1999 **ACM Computing Surveys (CSUR)**, Volume 31 Issue 4

Full text available: pdf(261.78 KB) Additional Information: full citation, abstract, references, citings, index terms

Transport layer protocols provide for end-to-end communication between two or more hosts. This paper presents a tutorial on transport layer concepts and terminology, and a survey of transport layer services and protocols. The transport layer protocol TCP is used as a reference point, and compared and contrasted with nineteen other protocols designed over the past two decades. The service and protocol features of twelve of the most important protocols are summarized in both text and tables.< ...

Keywords: TCP/IP networks, congestion control, flow control, transport protocol, transport service

13 From VHDL to efficient and first-time-right designs: a formal approach
Peter F. A. Middelhoek, Sreeranga P. Rajan
April 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 2

Full text available: pdf(722.99 KB) Additional Information: full citation, abstract, references, citings, index terms

In this article we provide a practical transformational approach to the synthesis of correct synchronous digital hardware designs from high-level specifications. We do this while taking into account the complete life cycle of a design from early prototype to full custom implementation. Besides time-to-market, both flexibility with respect to target architecture and efficiency issues are addressed by the methodology. The utilization of user-selected behavior-preserving transformation steps e ...

Keywords: CDFG, SFG, VHDL, correctness by construction, design methodology, rapid system prototyping, transformational design

14 Architectural considerations for a microprogrammable emulating engine using bit-slices
C. Halatsis, A. van Dam, J. Joosten, M. Letheren
May 1980 **Proceedings of the 7th annual symposium on Computer Architecture**

Full text available: pdf(951.32 KB) Additional Information: full citation, abstract, references, index terms

This paper describes architectural considerations which led to the design of a fast programmable processor made from ECL bit-slioes. The processor will be used as an on-line data filtering engine for high energy physics experiments. Unlike prior designs of such engines, the processor supports both user (horizontal) microcode and emulation of the PDP-11 fixed point instruction set (without memory management and multiple interrupt levels). In addition to an overview of the techniques used to ...

15 A Diagnostic Emulator for HEAO software development
Peter H. Beer, Kenneth J. Hupf
August 1976 **Proceedings of the fourth symposium on Simulation of computer systems**

Full text available: pdf(701.56 KB) Additional Information: full citation, abstract, references, index terms

Diagnostic Emulation is the application of microprogramming to the emulation of an operational computer to support software development and verification for that computer. A conventional technique, Interpretive Computer Simulation (ICS), has been used for many years in support of such software development and verification efforts. The ICS method is becoming less cost effective. For the development of attitude control software for NASA's High Energy Astronomical Observatory (HEAO) diagnostic ...

16 Implementation aspects of a SPARC V9 complete machine simulator

Bill Clarke, Adam Czezowski, Peter Strazdins
January 2002 **Australian Computer Science Communications , Proceedings of the twenty-fifth Australasian conference on Computer science - Volume 4**, Volume 24 Issue 1
Full text available: pdf(1.33 MB) Additional Information: full citation, abstract, references, index terms

In this paper we present work in progress in the development of a complete machine simulator for the UltraSPARC, an implementation of the SPARC V9 architecture. The complexity of the UltraSPARC ISA presents many challenges in developing a reliable and yet reasonably efficient implementation of such a simulator. Our implementation includes a heavily object-oriented design for the simulator modules and infrastructure, caching of repeated computations for performance, adding an OS (system call) emu ...

Keywords: SMP, SPARC V9 ISA, UltraSPARC, complete machine simulator, execution-driven simulation, object-oriented design

17 THEMIS logic simulator - a mix mode, multi-level, hierarchical, interactive digital circuit simulator
Mahesh H. Doshi, Roderick B. Sullivan, Donald M. Schuler
June 1984 **21st Proceedings of the Design Automation Conference on Design automation**
Full text available: pdf(764.43 KB) Additional Information: full citation, abstract, references, citings, index terms

A new logic simulator called THEMISTM Logic Simulator for the design of LSI, VLSI and PCBs is described. THEMIS supports design verification and test development from initial specification in behavioral and RTL languages to analysis of the final layout at the gate and switch level. To allow the simulation of an entire system or check the correctness of a single circuit, the different modeling techniques can be easily intermixed. THEMIS is a highly interactive simulator ...

18 Measuring the effects of internet path faults on reactive routing
Nick Feamster, David G. Andersen, Hari Balakrishnan, M. Frans Kaashoek
June 2003 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 2003 ACM SIGMETRICS international conference on Measurement and modeling of computer systems**, Volume 31 Issue 1
Full text available: pdf(394.56 KB) Additional Information: full citation, abstract, references, citings, index terms

Empirical evidence suggests that reactive routing systems improve resilience to Internet path failures. They detect and route around faulty paths based on measurements of path performance. This paper seeks to understand *why* and under *what circumstances* these techniques are effective.To do so, this paper correlates end-to-end active probing experiments, loss-triggered traceroutes of Internet paths, and BGP routing messages. These correlations shed light on three questions about Inte ...

19 HALSIM—a very fast SPARC V9 behavioral model
David Barach, Jaspal Kohli, John Slice, Marc Spaulding, Rajeev Bharadhwaj, Don Hudson, Cliff Neighbors, Nirmal Saxena, Rolland Crunk
March 1994 **ACM SIGARCH Computer Architecture News**, Volume 22 Issue 1
Full text available: pdf(586.68 KB) Additional Information: full citation, abstract, index terms

This paper describes several implementation techniques used in HAL's 250 KIPS SPARC V9 behavioral model. Beyond presenting the details of our processor model, we describe several areas of innovation: architectural state-vector capture for injection into a gate-level hardware model, using an EDC polynomial-based signature scheme to verify a hardware design; obtaining accurate kernel and user-mode instruction trace data.

20 ReEnact: using thread-level speculation mechanisms to debug data races in

multithreaded codes
Milos Prvulovic, Josep Torrellas
May 2003 **ACM SIGARCH Computer Architecture News , Proceedings of the 30th annual international symposium on Computer architecture**, Volume 31 Issue 2
Full text available: pdf(184.86 KB) Additional Information: full citation, abstract, references

While removing software bugs consumes vast amounts of human time, hardware support for debugging in modern computers remains rudimentary. Fortunately, we show that mechanisms for Thread-Level Speculation (TLS) can be reused to boost debugging productivity. Most notably, TLS's rollback capabilities can be extended to support rolling back recent buggy execution and repeating it as many times as necessary until the bug is fully characterized. These incremental re-executions are deterministic even i ...

Results 1 - 20 of 35 Result page: **1** 2 next

Terms used
emulation and **debug** and **clock** and **trigger** and **trace**

Found **35** of **807,214**

Sort results by: relevance
Display results: expanded form

Save results to a Binder
Search Tips
☐ Open results in a new window

Try an Advanced Search
Try this search in The Digital Library

Results 21 - 35 of 35 Result page: previous 1 **2**

Relevance scale

21 Simulating modular microcomputers
Frank J. Langley, Gerald A. LaGro, Joan Sheehan
March 1978 **Proceedings of the eleventh annual simulation symposium**

Full text available: pdf(1.47 MB) Additional Information: full citation, abstract, references, citings, index terms

The commitment of microprocessor-based system configurations to detailed logic design and breadboard fabrication traditionally results in a costly development cycle. This paper reports on the use of a computer design high-order-language (HOL) to simulate micro-computer functional elements, "macromodules", at the register level, and verify the timing and interface requirements for a family of microcomputer configurations. The definitions of these microcomputer macromodules (i. e. ...

22 EASY—an operating system for the QM-1
Charles W. Flink
October 1977 **Proceedings of the 10th annual workshop on Microprogramming**

Full text available: pdf(733.19 KB) Additional Information: full citation, abstract, references, citings, index terms

The Emulation Aid SYstem is a virtual machine monitor for the Nanodata QM-1 microprogrammable computer. The system is designed to provide the user with an interactive interface for the development and subsequent use of emulations on the QM-1. EASY provides integrated support for: 1) interactive control of multiple, concurrently resident, virtual computers implemented via emulation, 2) input/output from emulations (virtual I/O) to the various real peripherals of the QM-1, and 3) diagnostic d ...

Keywords: Emulation, Intermediate language machines, Microprogramming, Nanodata QM-1, Software engineering, Virtual machine monitors, Virtual machines

23 Report on the Second European SIGOPS Workshop "making distributed systems work"
Sape Mullender
January 1987 **ACM SIGOPS Operating Systems Review**, Volume 21 Issue 1

Full text available: pdf(1.89 MB) Additional Information: full citation, index terms

24 A structural view of the Cedar programming environment
Daniel C. Swinehart, Polle T. Zellweger, Richard J. Beach, Robert B. Hagmann

August 1986 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 8 Issue 4

Full text available: pdf(6.32 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents an overview of the Cedar programming environment, focusing on its overall structure—that is, the major components of Cedar and the way they are organized. Cedar supports the development of programs written in a single programming language, also called Cedar. Its primary purpose is to increase the productivity of programmers whose activities include experimental programming and the development of prototype software systems for a high-performance personal computer. T ...

25 Performance monitoring for multiprocessor networks

Rebecca E. Adams

April 1979 **Proceedings of the 17th annual Southeast regional conference**

Full text available: pdf(124.61 KB) Additional Information: full citation

26 A real-time support processor for ada tasking

J. Roos

April 1989 **ACM SIGARCH Computer Architecture News , Proceedings of the third international conference on Architectural support for programming languages and operating systems**, Volume 17 Issue 2

Full text available: pdf(978.85 KB) Additional Information: full citation, abstract, references, citings, index terms

Task synchronization in Ada causes excessive run-time overhead due to the complex semantics of the rendezvous. To demonstrate that the speed can be increased by two orders of magnitude by using special purpose hardware, a single chip VLSI support processor has been designed. By providing predictable and uniformly low overhead for the entire semantics of a rendezvous, the powerful real-time constructs of Ada can be used freely without performance degradation. The key to high perfo ...

27 Statemate: a working environment for the development of complex reactive systems

D. Harel, H. Lachover, A. Naamad, A. Pnueli, M. Politi, R. Sherman, a. Shtul-Trauring

April 1988 **Proceedings of the 10th international conference on Software engineering**

Full text available: pdf(1.19 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper provides a brief overview of the STATEMATE system, constructed over the past three years by i-Logix Inc., and Ad Cad Ltd. STATEMATE is a graphical working environment, intended for the specification, analysis, design and documentation of large and complex reactive systems, such as real-time embedded systems, control and communication systems, and interactive software. It enables a user to prepare, analyze and debug diagrammatic, yet precise, descriptions of the system under devel ...

28 The structure of Cedar

Daniel C. Swinehart, Polle T. Zellweger, Robert B. Hagmann

June 1985 **Proceedings of the ACM SIGPLAN 85 symposium on Language issues in programming environments**, Volume 20 , 18 Issue 7 , 6

Full text available: pdf(1.79 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents an overview of the Cedar programming environment, focusing primarily on its overall structure: the major components of Cedar and the way they are organized. Cedar supports the development of programs written in a single programming language, also called Cedar. We will emphasize the extent to which the Cedar language, with runtime support, has influenced the organization, comprehensibility, and stability of Cedar. Produced in the Computer Science Laboratory (CS ...

29 Robustness: CMC: a pragmatic approach to model checking real code
Madanlal Musuvathi, David Y. W. Park, Andy Chou, Dawson R. Engler, David L. Dill
December 2002 **ACM SIGOPS Operating Systems Review**, Volume 36 Issue SI

Full text available: pdf(1.55 MB) Additional Information: full citation, abstract, references

Many system errors do not emerge unless some intricate sequence of events occurs. In practice, this means that most systems have errors that only trigger after days or weeks of execution. Model checking [4] is an effective way to find such subtle errors. It takes a simplified description of the code and exhaustively tests it on all inputs, using techniques to explore vast state spaces efficiently. Unfortunately, while model checking systems code would be wonderful, it is almost never done in pra ...

30 RFC2000: Internet Official Protocol Standards
February 1997 rfc, RFC Editor

Additional Information: full citation

31 IPwatch: a tool for monitoring network locality
Mark J. Lorence, M. Satyanarayanan
January 1990 **ACM SIGOPS Operating Systems Review**, Volume 24 Issue 1

Full text available: pdf(1.18 MB) Additional Information: full citation, abstract, citings, index terms

In this paper we introduce the concepts of *Logical* and *Physical Network Locality* and point out their importance to the performance of distributed systems. We then describe the design of *IPwatch*, a simple and inexpensive tool for monitoring logical network locality. IPwatch exploits short-term locality to enable monitoring of medium- and long-term locality of large networks using modest computational resources. We describe experiments at Carnegie Mellon University to validate ...

32 High level hierarchical fault simulation techniques
William A. Rogers, Jacob A. Abraham
March 1985 **Proceedings of the 1985 ACM thirteenth annual conference on Computer Science**

Full text available: pdf(1.05 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents techniques for simulating directly from a hierarchical circuit description without flattening to the level of primitives. An overview of traditional fault simulation techniques is followed by details of the hierarchical techniques. The fault model is shown to be decoupled from the simulator programs through the use of a fault library. The fault library allows the user to mix both functional and technology-dependent fault models, which allows fault simulation and conseque ...

33 RFC2200: Internet Official Protocol Standards
J. Postel
June 1997 rfc, RFC Editor

Additional Information: full citation

34 Functional verification of a multiple-issue, out-of-order, superscalar Alpha processor—the DEC Alpha 21264 microprocessor
Scott Taylor, Michael Quinn, Darren Brown, Nathan Dohm, Scot Hildebrandt, James Huggins, Carl Ramey
May 1998 **Proceedings of the 35th annual conference on Design automation conference**

Full text available: pdf(153.68 KB) Additional Information: full citation, abstract, references, citings, index

terms

DIGITAL's Alpha 21264 processor is a highly out-of-order, superpipelined, superscalar implementation of the Alpha architecture, capable of a peak execution rate of six instructions per cycle and a sustainable rate of four per cycle. The 21264 also features a 500 MHz clock speed and a high-bandwidth system interface that channels up to 5.3 Gbytes/second of cache data and 2.6 Gbytes/second of main-memory data into the processor. Simulation-based functional verification was performed on the Io ...

Keywords: 21264, Alpha, architecture, coverage anaysis, microprocessor, pseudo-random, validation, verification

35 Advances in functional abstraction from structure

Richard H. Lathrop, Robert J. Hall, Gavan Duffy, K. Mark Alexander, Robert S. Kirk
June 1988 **Proceedings of the 25th ACM/IEEE conference on Design automation**

Full text available: pdf(537.20 KB) Additional Information: full citation, abstract, references, index terms

FUNSTRUX has been extended to extract behavioral level models for a commercial simulator directly from a circuit netlist. Recent advances include: a retargetable code generation mechanism; an object-oriented control structure; handling of initialization values; and improved run-time and space requirements of the abstraction process. We discuss some of the issues that arise in translating from LISP to 'C' and from one functional paradigm to another.

Results 21 - 35 of 35 Result page: previous 1 **2**

- **June 5th 0500gmt-1300gmt**: DataStar Web will be down for software/hardware maintenance

Dialog DataStar

options | logoff | feedback | help

databases | search page

Titles

To view one or many selected titles scroll down the list and click the corresponding boxes. Then click display at the b page. To view one particular document click the link above the title to display immediately.

Documents 1 to 4 of 4 from your search **"emulation AND debug AND clock"** in all the available information:
Number of titles selected from other pages: 0

☐ **Select All**

☐ 1 display full document

2001. (INZZ) A hardware accelerator for DSP system design: University of Tehran DSP Hardware Emulator (UTDHE).

☐ 2 display full document

1998. (INZZ) A 200 MHz 1.2 W 1.4 GFLOPS microprocessor with graphic operation unit.

☐ 3 display full document

1996. (INZZ) Device for debugging IBM PC extender cards.

☐ 4 display full document

1993. (INZZ) Pattern generator card, **emulation,** and **debug.**

Selection	Display Format	Display in	ERA SM Electronic Redistribution & Archivin
◉ from this page ○ from all pages	◉ Full ○ Free ○ Short ○ Medium ○ Custom Help with Formats	◉ HTML ○ Tagged (for tables)	Copies you will redistribute: [ ] Employees who will access archived record (s): [ ] Help with ERA

Sort your entire search result by Publication year | Ascending

Top - News & FAQS - Dialog

WEST Search History

Hide Items | Restore | Clear | Cancel

DATE: Thursday, June 03, 2004

Hide?	Set Name	Query	Hit Count
	DB=PGPB,USPT; THES=ASSIGNEE; PLUR=YES; OP=ADJ		
☐	L12	L11 and RDI	4
☐	L11	L10 and emulation	95
☐	L10	real time debug	130
☐	L9	L8 and test	24
☐	L8	L7 and synchron$	24
☐	L7	L6 and trace trigger	35
☐	L6	L5 and (integrated circuit or IC)	89
☐	L5	L4 and trace	97
☐	L4	L3 and oscillator	128
☐	L3	L2 and trigger	464
☐	L2	L1 and clock	970
☐	L1	emulation and debug	1413

END OF SEARCH HISTORY

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 4 of 4 returned.

☐ 1. Document ID: US 6738929 B2

Using default format because multiple data bases are involved.

L12: Entry 1 of 4 File: USPT May 18, 2004

US-PAT-NO: 6738929
DOCUMENT-IDENTIFIER: US 6738929 B2

TITLE: Dynamically configurable debug port for concurrent support of debug functions from multiple data processing cores

DATE-ISSUED: May 18, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Swoboda; Gary L.	Sugar Land	TX		
Deao; Douglas E.	Sugar Land	TX		

US-CL-CURRENT: 714/28; 714/25, 714/27, 714/30, 714/31, 714/32, 714/33, 714/37, 714/39, 714/40, 714/45, 714/46

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

☐ 2. Document ID: US 6725391 B2

L12: Entry 2 of 4 File: USPT Apr 20, 2004

US-PAT-NO: 6725391
DOCUMENT-IDENTIFIER: US 6725391 B2

TITLE: Clock modes for a debug port with on the fly clock switching

DATE-ISSUED: April 20, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Swoboda; Gary L.	Sugarland	TX		

US-CL-CURRENT: 713/500; 713/400, 713/501, 714/28, 714/731

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw De

☐ 3. Document ID: US 6545549 B2

L12: Entry 3 of 4 File: USPT Apr 8, 2003

US-PAT-NO: 6545549
DOCUMENT-IDENTIFIER: US 6545549 B2

TITLE: Remotely controllable phase locked loop clock circuit

DATE-ISSUED: April 8, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Swoboda; Gary L.	Sugarland	TX		

US-CL-CURRENT: 331/18; 327/156, 327/159, 331/1A, 331/16, 331/25, 331/57

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw D

☐ 4. Document ID: US 6388533 B1

L12: Entry 4 of 4 File: USPT May 14, 2002

US-PAT-NO: 6388533
DOCUMENT-IDENTIFIER: US 6388533 B1

TITLE: Programmable ring oscillator

DATE-ISSUED: May 14, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Swoboda; Gary L.	Sugarland	TX		

US-CL-CURRENT: 331/57; 331/1A, 331/17, 331/179

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw D

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
RDI	925
RDIS	57
(RDI AND 11).PGPB,USPT.	4
(L11 AND RDI).PGPB,USPT.	4

Display Format: - Change Format

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 1 through 20 of 24 returned.

☐ 1. Document ID: US 20040103400 A1

Using default format because multiple data bases are involved.

L9: Entry 1 of 24 File: PGPB May 27, 2004

PGPUB-DOCUMENT-NUMBER: 20040103400
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040103400 A1

TITLE: Recovery from corruption using event offset format in data trace

PUBLICATION-DATE: May 27, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Johnsen, John M.	Dallas	TX	US	
Agarwala, Manisha	Richardson	TX	US	
Gill, Maria B. H.	Plano	TX	US	

US-CL-CURRENT: 717/128; 709/238, 714/25, 717/177

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw D

☐ 2. Document ID: US 20040103399 A1

L9: Entry 2 of 24 File: PGPB May 27, 2004

PGPUB-DOCUMENT-NUMBER: 20040103399
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040103399 A1

TITLE: Data trace compression map

PUBLICATION-DATE: May 27, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Agarwala, Manisha	Richardson	TX	US	
Thome, Bryan	Missouri City	TX	US	
Johnsen, John M.	Dallas	TX	US	
Swoboda, Gary L.	Sugarland	TX	US	
Nardini, Lewis	Dallas	TX	US	
Gill, Maria B. H.	Plano	TX	US	

US-CL-CURRENT: 717/128; 709/238

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

---

☐ 3. Document ID: US 20040103397 A1

L9: Entry 3 of 24 File: PGPB May 27, 2004

PGPUB-DOCUMENT-NUMBER: 20040103397
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040103397 A1

TITLE: Maintaining coherent synchronization between data streams on detection of overflow

PUBLICATION-DATE: May 27, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Agarwala, Manisha	Richardson	TX	US	
Johnsen, John M.	Dallas	TX	US	

US-CL-CURRENT: 717/128; 709/238, 717/177

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

---

☐ 4. Document ID: US 20040103349 A1

L9: Entry 4 of 24 File: PGPB May 27, 2004

PGPUB-DOCUMENT-NUMBER: 20040103349
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040103349 A1

TITLE: Programmable extended compression mask for dynamic trace

PUBLICATION-DATE: May 27, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Nardini, Lewis	Dallas	TX	US	
Agarwala, Manisha	Richardson	TX	US	
Johnsen, John M	Dallas	TX	US	

US-CL-CURRENT: 714/39

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

---

☐ 5. Document ID: US 20040102954 A1

L9: Entry 5 of 24 File: PGPB May 27, 2004

PGPUB-DOCUMENT-NUMBER: 20040102954
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040102954 A1

TITLE: Dynamic data trace output scheme

PUBLICATION-DATE: May 27, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Agarwala, Manisha	Richardson	TX	US	
Gill, Maria B. H.	Plano	TX	US	
Johnsen, John M.	Dallas	TX	US	

US-CL-CURRENT: 703/28

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw D

☐ 6. Document ID: US 20040102953 A1

L9: Entry 6 of 24 File: PGPB May 27, 2004

PGPUB-DOCUMENT-NUMBER: 20040102953
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040102953 A1

TITLE: Trigger ordering for trace streams when multiple triggers accumulate

PUBLICATION-DATE: May 27, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Agarwala, Manisha	Richardson	TX	US	
Johnsen, John M.	Dallas	TX	US	
Nardini, Lewis	Dallas	TX	US	

US-CL-CURRENT: 703/24

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWMC | Draw D

☐ 7. Document ID: US 20040102952 A1

L9: Entry 7 of 24 File: PGPB May 27, 2004

PGPUB-DOCUMENT-NUMBER: 20040102952
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040102952 A1

TITLE: Multi-port trace data handling

PUBLICATION-DATE: May 27, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Agarwala, Manisha	Richardson	TX	US	
Nardini, Lewis	Dallas	TX	US	
Johnsen, John M.	Dallas	TX	US	
Gill, Maria B. H.	Plano	TX	US	
Flores, Jose L.	Richardson	TX	US	

US-CL-CURRENT: 703/23

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

---

☐ 8. Document ID: US 20040102951 A1

L9: Entry 8 of 24 File: PGPB May 27, 2004

PGPUB-DOCUMENT-NUMBER: 20040102951
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040102951 A1

TITLE: Read FIFO scheduling for multiple streams while maintaining coherency

PUBLICATION-DATE: May 27, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Agarwala, Manisha	Richardson	TX	US	
Gill, Maria B.H.	Plano	TX	US	

US-CL-CURRENT: 703/23

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

---

☐ 9. Document ID: US 20040102950 A1

L9: Entry 9 of 24 File: PGPB May 27, 2004

PGPUB-DOCUMENT-NUMBER: 20040102950
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040102950 A1

TITLE: Stalling CPU pipeline to prevent corruption in trace while maintaining coherency with asynchronous events

PUBLICATION-DATE: May 27, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Agarwala, Manisha	Richardson	TX	US	
Johnsen, John M.	Dallas	TX	US	

US-CL-CURRENT: 703/23

☐ 10. Document ID: US 20020111785 A1

L9: Entry 10 of 24 File: PGPB Aug 15, 2002

PGPUB-DOCUMENT-NUMBER: 20020111785
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020111785 A1

TITLE: Synchronizing on-chip data processor trace and timing information for export

PUBLICATION-DATE: August 15, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Swoboda, Gary L.	Sugar Land	TX	US	
McGowan, Robert A.	Monroeville	PA	US	

US-CL-CURRENT: 703/28

☐ 11. Document ID: US 20020069042 A1

L9: Entry 11 of 24 File: PGPB Jun 6, 2002

PGPUB-DOCUMENT-NUMBER: 20020069042
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020069042 A1

TITLE: Collecting and exporting on-chip data processor trace and timing information with differing collection and export formats

PUBLICATION-DATE: June 6, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Swoboda, Gary L.	Sugar Land	TX	US	

US-CL-CURRENT: 703/19; 703/14

☐ 12. Document ID: US 20020065642 A1

L9: Entry 12 of 24 File: PGPB May 30, 2002

PGPUB-DOCUMENT-NUMBER: 20020065642
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020065642 A1

TITLE: Using selective omission to compress on-chip data processor trace and timing

information for export

PUBLICATION-DATE: May 30, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Swoboda, Gary L.	Sugar Land	TX	US	

US-CL-CURRENT: 703/19

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

---

☐ 13. Document ID: US 20020055831 A1

L9: Entry 13 of 24 File: PGPB May 9, 2002

PGPUB-DOCUMENT-NUMBER: 20020055831
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020055831 A1

TITLE: Using sign extension to compress on-chip data processor trace and timing information for export

PUBLICATION-DATE: May 9, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Swoboda, Gary L.	Sugar Land	TX	US	

US-CL-CURRENT: 703/19

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

---

☐ 14. Document ID: US 20020055830 A1

L9: Entry 14 of 24 File: PGPB May 9, 2002

PGPUB-DOCUMENT-NUMBER: 20020055830
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020055830 A1

TITLE: Correlating on-chip data processor trace information for export

PUBLICATION-DATE: May 9, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Swoboda, Gary L.	Sugar Land	TX	US	
McGowan, Robert A.	Monroeville	PA	US	

US-CL-CURRENT: 703/19

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 15. Document ID: US 20020055828 A1

L9: Entry 15 of 24 File: PGPB May 9, 2002

PGPUB-DOCUMENT-NUMBER: 20020055828
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020055828 A1

TITLE: Exporting on-chip data processor trace information with variable proportions of control and data

PUBLICATION-DATE: May 9, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Swoboda, Gary L.	Sugar Land	TX	US	
McGowan, Robert A.	Monroeville	PA	US	

US-CL-CURRENT: 703/13

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. De

☐ 16. Document ID: US 20020035721 A1

L9: Entry 16 of 24 File: PGPB Mar 21, 2002

PGPUB-DOCUMENT-NUMBER: 20020035721
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020035721 A1

TITLE: Clock modes for a debug port with on the fly clock switching

PUBLICATION-DATE: March 21, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Swoboda, Gary L.	Sugarland	TX	US	

US-CL-CURRENT: 717/128

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. De

☐ 17. Document ID: US 20020008591 A1

L9: Entry 17 of 24 File: PGPB Jan 24, 2002

PGPUB-DOCUMENT-NUMBER: 20020008591
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020008591 A1

TITLE: Programmable ring oscillator

PUBLICATION-DATE: January 24, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Swoboda, Gary L.	Sugarland	TX	US	

US-CL-CURRENT: 331/57; 331/177R, 331/DIG.3

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

---

☐ 18. Document ID: US 20020007264 A1

L9: Entry 18 of 24 File: PGPB Jan 17, 2002

PGPUB-DOCUMENT-NUMBER: 20020007264
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020007264 A1

TITLE: Debug bi-phase export and data recovery

PUBLICATION-DATE: January 17, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Swoboda, Gary L.	Sugarland	TX	US	

US-CL-CURRENT: 703/28

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

---

☐ 19. Document ID: US 20020006451 A1

L9: Entry 19 of 24 File: PGPB Jan 17, 2002

PGPUB-DOCUMENT-NUMBER: 20020006451
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020006451 A1

TITLE: Debug output loosely coupled with processor block

PUBLICATION-DATE: January 17, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Swoboda, Gary L.	Sugarland	TX	US	
McGowan, Robert A.	Monroeville	PA	US	

US-CL-CURRENT: 425/67; 425/313, 425/464

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

---

☐ 20. Document ID: US 20010043122 A1

L9: Entry 20 of 24 File: PGPB Nov 22, 2001

PGPUB-DOCUMENT-NUMBER: 20010043122
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010043122 A1

TITLE: Remotely controllable phase locked loop clock circuit

PUBLICATION-DATE: November 22, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Swoboda, Gary L.	Sugarland	TX	US	

US-CL-CURRENT: 331/18; 331/25

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. De

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
TEST	743954
TESTS	355548
(8 AND TEST).PGPB,USPT.	24
(L8 AND TEST).PGPB,USPT.	24

Display Format: - Change Format

Previous Page Next Page Go to Doc#

Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 21 through 24 of 24 returned.

☐ 21. Document ID: US 20010034597 A1

Using default format because multiple data bases are involved.

L9: Entry 21 of 24 File: PGPB Oct 25, 2001

PGPUB-DOCUMENT-NUMBER: 20010034597
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20010034597 A1

TITLE: Obtaining and exporting on-chip data processor trace and timing information

PUBLICATION-DATE: October 25, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Swoboda, Gary L.	Sugar Land	TX	US	
McGowan, Robert A.	Monroeville	PA	US	

US-CL-CURRENT: 703/26

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 22. Document ID: US 6725391 B2

L9: Entry 22 of 24 File: USPT Apr 20, 2004

US-PAT-NO: 6725391
DOCUMENT-IDENTIFIER: US 6725391 B2

TITLE: Clock modes for a debug port with on the fly clock switching

DATE-ISSUED: April 20, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Swoboda; Gary L.	Sugarland	TX		

US-CL-CURRENT: 713/500; 713/400, 713/501, 714/28, 714/731

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 23. Document ID: US 6545549 B2

L9: Entry 23 of 24 File: USPT Apr 8, 2003

US-PAT-NO: 6545549
DOCUMENT-IDENTIFIER: US 6545549 B2

TITLE: Remotely controllable phase locked loop clock circuit

DATE-ISSUED: April 8, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Swoboda; Gary L.	Sugarland	TX		

US-CL-CURRENT: 331/18; 327/156, 327/159, 331/1A, 331/16, 331/25, 331/57

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

---

☐ 24. Document ID: US 6388533 B1

L9: Entry 24 of 24 File: USPT May 14, 2002

US-PAT-NO: 6388533
DOCUMENT-IDENTIFIER: US 6388533 B1

TITLE: Programmable ring oscillator

DATE-ISSUED: May 14, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Swoboda; Gary L.	Sugarland	TX		

US-CL-CURRENT: 331/57; 331/1A, 331/17, 331/179

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

---

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Term	Documents
TEST	743954
TESTS	355548
(8 AND TEST).PGPB,USPT.	24
(L8 AND TEST).PGPB,USPT.	24

Display Format: - Change Format

Previous Page Next Page Go to Doc#